What is claimed is:

1. A structure of mask read only memory, comprising:

a semiconductor structure having a first dielectric layer thereon, a plurality of buried bit lines and a plurality of code areas within said semiconductor structure, wherein each of said plurality of code areas is placed between two of plurality of said buried bit lines;

a second dielectric layer having a contact plug being placed on said semiconductor structure, wherein said contact plug comprises a first metal layer therein and a first glue layer thereon;

a second glue layer being on said second dielectric layer and said contact plug;

a second metal layer being on said second glue layer; and

a pad layer being on said second metal layer.

2. The structure of mask read only memory according to claim 1, wherein said first dielectric layer is above said plurality of buried bit lines.

3. The structure of mask read only memory according to claim 1, wherein said first metal layer is filled in said contact plug.

4. The structure of mask read only memory according to claim 1, wherein the material of said first metal layer is tungsten.

5. The structure of mask read only memory according to claim 1, wherein the material of said second dielectric layer is Borophosphosilicate Glass (BPSG).

6. The structure of mask read only memory according to claim 1, wherein the material of said first glue layer is titanium/titanium nitride (Ti/TiN).

7. The structure of mask read only memory according to claim 1, wherein said second glue layer comprises linear titanium/titanium nitride (Ti/TiN).

8. A method of manufacturing a mask read only memory, comprising:

providing a semiconductor structure having a first opening therein;

forming a first glue layer on a surface of said semiconductor structure extending into said first opening;

forming a contact plug within said semiconductor structure, said contact plug comprises a first metal layer therein and a first glue layer thereon;

etching said first glue layer outside said contact plug in order to expose said surface of said semiconductor structure;

forming a patterned photoresist layer on said semiconductor structure;

forming a plurality of code areas in said semiconductor structure by using said patterned photoresist layer as a mask;

removing said patterned photoresist layer; and

forming a second glue layer on said semiconductor structure.

9. The method of claim 8, wherein said semiconductor structure comprises a plurality of buried bit lines therein and a first dielectric layer thereon.

10. The method of claim 9,wherein each of said plurality of code areas is formed between two of said buried bit lines.

11. The method of claim 8, wherein said first metal layer is deposited to cover said first glue layer.

12. The method of claim 11, wherein said contact plug is formed by planarizing said first metal layer.

13. The method of claim 8, wherein the material of said first metal layer is tungsten.

14. The method of claim 8, wherein said etching said first glue layer outside said contact plug in order to expose said surface of said semiconductor structure comprises a blanket etching back process.

15. The method of claim 8, wherein said forming said plurality of code areas in said semiconductor structure by using an ion implantation process.

16. The method of claim 8, wherein the material of said second dielectric layer is Borophosphosilicate Glass (BPSG).

17. The method of claim 8, wherein the material of said first glue layer is titanium/titanium nitride (Ti/TiN).

18. The method of claim 8, wherein said second glue layer comprises linear titanium/titanium nitride (Ti/TiN).

19. A method of manufacturing a mask read only memory, comprising:

providing a semiconductor structure having a plurality of buried bit lines therein and a first dielectric layer thereon;

forming a second dielectric layer on said first dielectric layer;

forming a first opening within said second dielectric layer, and exposing a portion of said first dielectric layer;

forming a first glue layer on said surface of said second dielectric layer and on a side-wall and bottom of said first opening;

forming a contact plug within said second dielectric layer;

blanket etching back said first glue layer outside said contact plug in order to expose a surface of said second dielectric layer;

forming a photoresist layer having a second opening therein and on said second dielectric layer, wherein said second opening being centered between two of said plurality of buried bit lines;

ion implanting to form a plurality of code areas in said semiconductor structure and between two of said plurality of buried bit lines through said photoresist layer;

removing said photoresist layer;

forming a second glue layer on said second dielectric layer and on said contact plug;

depositing a second metal layer on said second glue layer; and

depositing a pad layer having a third opening therein and on said second metal layer.

20. The method of claim 19, further comprising a first metal layer is deposited to cover said first glue layer.

21. The method of claim 20, wherein said contact plug is formed by planarizing said first metal layer.

22. The method of claim 20, wherein the material of said first metal layer is tungsten.

23. The method of claim 19, wherein the material of said second dielectric layer is Borophosphosilicate Glass (BPSG).